Application Note

Document No.: AN1168

G32A1085 A1065 A1045

Application Guidelines

Version: V1.1

1 Introduction

This application note outlines critical design considerations for applications using the G32A1085 A1065 A1045 series.

Content

2 Hardware Application Design Notes

2.1 MCU Filter Capacitor Design

The MCU power supply pins, VDD and VSS, must be connected in parallel with both bulk and bypass capacitors. Refer to Figure 1 and Figure 2. In the figures, N indicates the number of VDD pins in each package. Capacitor performance depends strongly on placement and connection method. The PCB layout should use star routing so that the external power supply passes through the bulk and bypass capacitors before reaching the MCU. Place the filter capacitors as close to the MCU pins as possible, preferably within 4mm.

The 0Ω resistor in Figure 1 may be replaced with a ferrite bead to improve the EMI radiated emission (RE) margin. Recommended reference value: 600Ω@100MHz.

Figure 1 LQFP64/LQFP48 Filter Capacitor Design

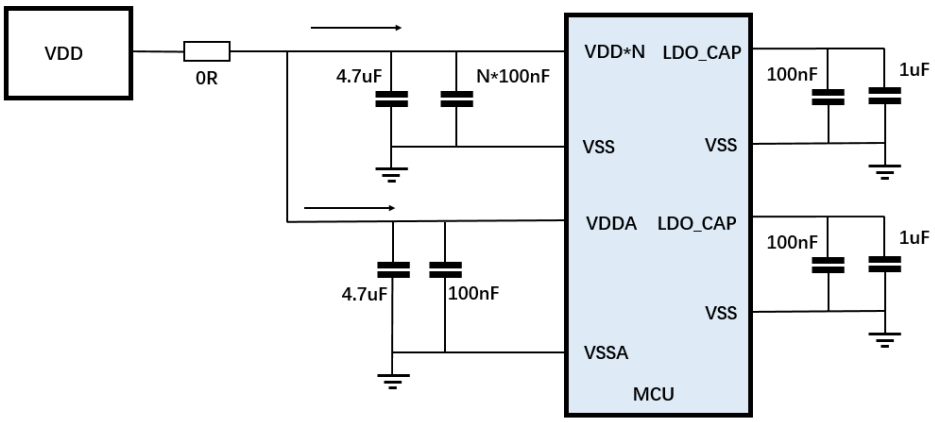
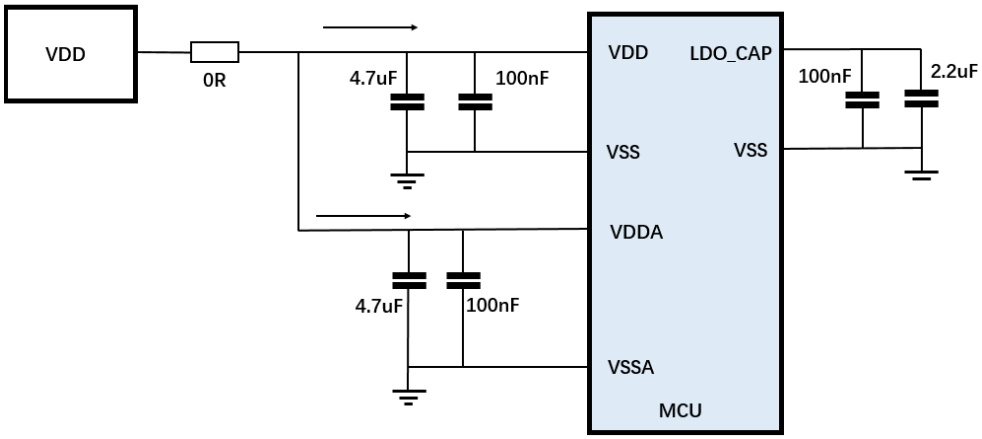


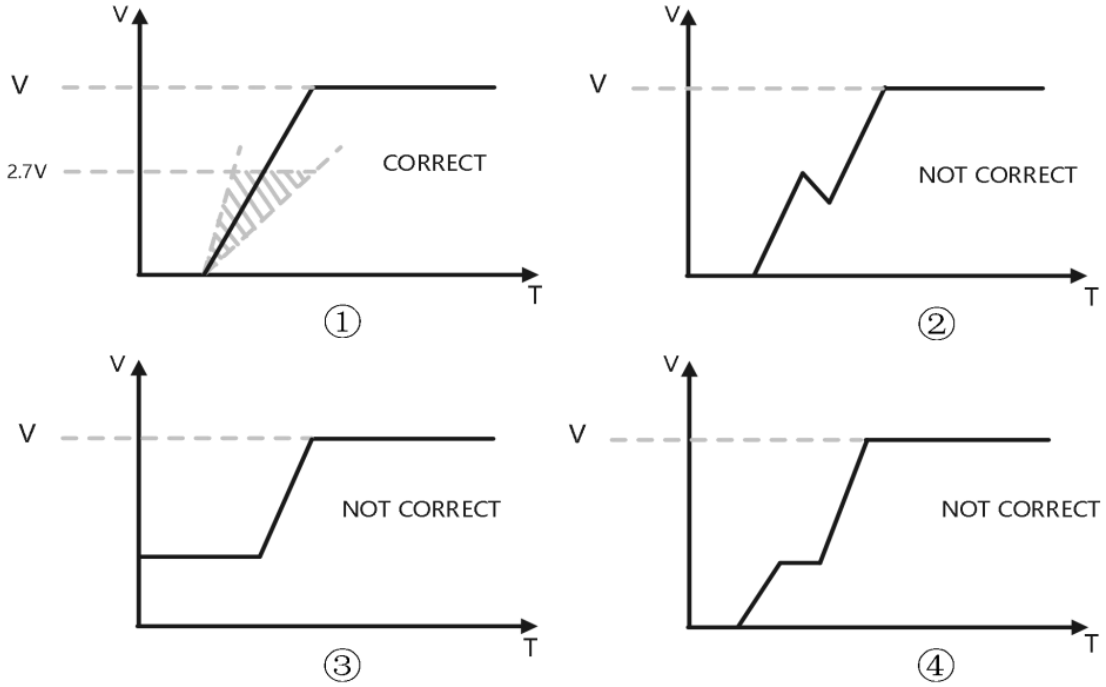
Figure 2 QFN32 Filter Capacitor Design



2.2 MCU Power Supply Notes

The MCU power supply ramp rate must meet the limits specified in the datasheet: greater than 0.5V/min and less than 100V/ms. The rise time from 0V to 5.5V must be at least 55μs, and the rise time from 0V to 2.7V must be at least 27μs. If the power-up ramp is too fast or too slow, the MCU may not operate correctly. Before power is applied again, VDD must first fall below 300mV. These timing requirements must be met across the full operating temperature range. The power-on waveform must match waveform ① in Figure 3; the other three waveforms are invalid.

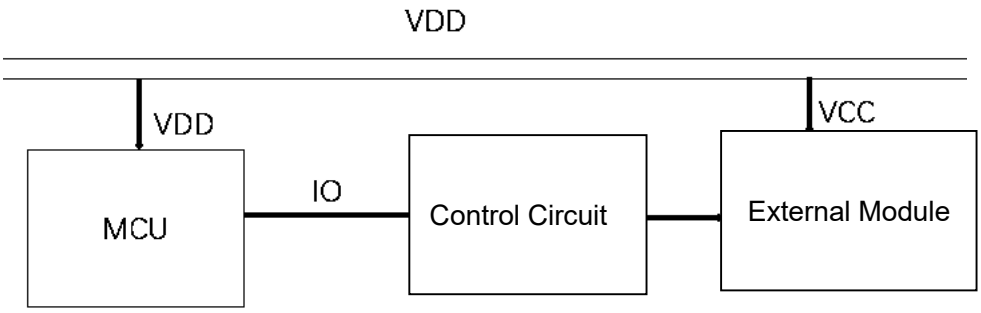
Figure 3 Power-On Waveform



2.3 Peripheral Modules Use VDD, VSS

When the MCU controls the power supply or power-up sequence of external modules, avoid fast power-up transitions that may cause surge current and pull down VDD. Use proper delays to ensure smooth power transitions, stable system operation, and circuit protection. Buffer components, such as capacitors or resistors, may be added to slow the power-up rate and prevent VDD from dropping due to instantaneous high current demand. If VDD does drop, its fall rate must still meet the ECU power supply ramp-rate requirement. See the usage examples in Figure 4 and Figure 5.

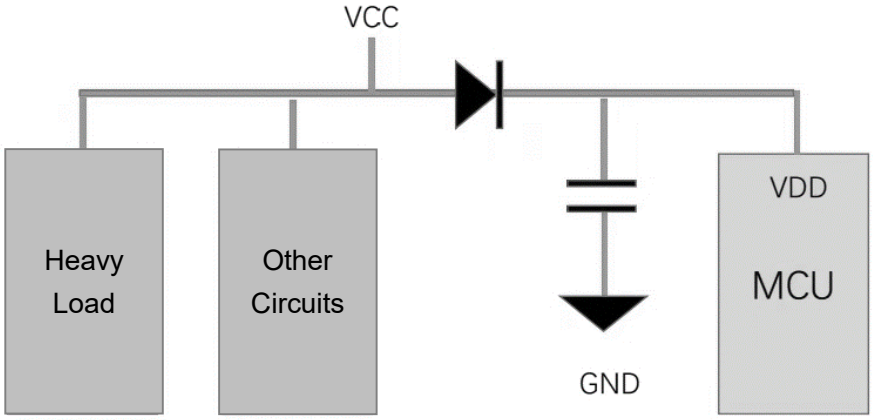
Figure 4 IO-Controlled Peripheral Module



For applications where the MCU supply voltage exceeds 3.6V, add protection against supply fluctuations. This can be done by adding a low-dropout diode in series, or by using a 10Ω series resistor with a capacitor of at least 10μF in parallel, forming a fast power-loss protection circuit. With a sufficiently large capacitor, power-down becomes slower, and the voltage drop is reduced. In Figure 4, buffer components are added to the control circuit. In Figure 5, heavy loads are separated from the MCU supply, and buffer components are used to form the fast power-loss protection circuit.

For example, a germanium diode produces about a 0.2V forward voltage drop when conducting, reducing the MCU supply voltage by 0.2V. If the ADC or DAC is used, this voltage drop may affect accuracy.

Figure 5 Peripheral Shared Power Supply



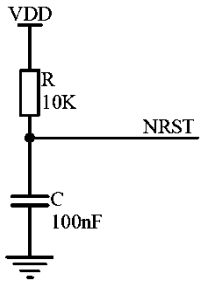
2.4 NRST Pin Pull-Up and Filter Capacitor Notes

The NRST pin must not be connected to a strong external pull-up. If an external pull-up resistor is used, its value must be greater than 1kΩ; 10kΩ is recommended. A smaller resistance may affect the startup.

If NRST is connected to another controller or debugger, check whether that device has an internal pull-up. If the internal pull-up resistance is low, add a series resistor of several hundred ohms; 200Ω is recommended to reduce external interference.

If an external filter capacitor is connected to NRST, 100nF is recommended. The capacitance must not exceed 500nF, because a larger value may affect the windowed watchdog function.

Figure 6 Reset Circuit



2.5 External and High-Frequency Signals

For signals such as zero-crossing signals, relay signals, and AC load signals, check whether they may cause sudden load increases. Bypass capacitors can be used to reduce load transients.

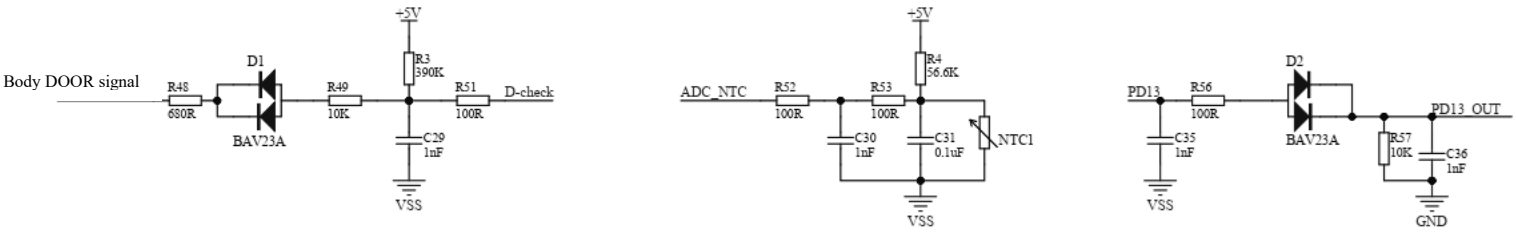
For high-frequency signal lines, such as I2C clock, SPI clock, CANH, and CANL, check whether instantaneous spike currents may be generated.

2.6 I/O Port Series Resistors and Bypass Capacitors

For input/output ports, including ADC inputs, external interrupts, and communication interfaces, add series protection resistors in the circuit design where appropriate. Select the resistor value so that the theoretical maximum current does not exceed the absolute maximum rating of the MCU port. Place both the series resistor and the parallel capacitor as close to the MCU pin as possible. The series resistor must be placed before the parallel capacitor. The ground of the peripheral module filter capacitor must connect to the ground node after the VDD/VSS bulk and bypass capacitors. Figure 7 shows an example resistor-capacitor connection for a body DOOR signal, ADC detection, and IO_OUT, using a 100Ω series resistor and a 1nF capacitor to VSS on the IO port.

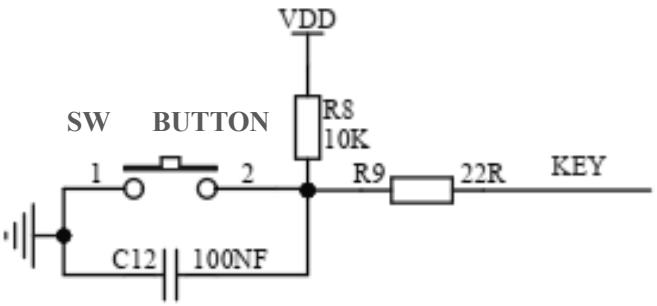
Note: In PCB designs with interconnected modules, such as separated lighting and control modules or separated sensor and control modules, the series resistors and parallel capacitors must be placed on the MCU PCB. Correct component values and placement help prevent ESD/EOS damage to MCU ports.

Figure 7 Circuit Example for Body DOOR Signal/ADC Detection/IO_OUT



For button circuits, the following design is recommended:

Figure 8 Button Circuit



For C12 in Figure 7, a 100nF capacitor is recommended. Use a small series resistor R9, such as 22Ω, 100Ω, or 1kΩ. In the PCB layout, place capacitor C12 as close to button SW as possible to suppress the negative voltage spike generated during button actuation.

2.7 IO Voltage Must Not Exceed VDD

If the IC has no VDD supply but an IO pin is driven by an external voltage, the IC may be powered through the IO clamp protection diode. Similarly, if the IC is powered but an IO pin voltage is higher than VDD, the voltage difference may forward-bias the clamp diode and inject current into VDD. Under normal operating conditions, the IO voltage must not exceed VDD by more than 0.3V.

This condition may cause the following issues:

(1) Excessive current may overload and damage the IO clamp diode.

(2) The MCU may fail to reset correctly.

(3) The program may run abnormally.

(4) Latch-up may occur.

2.8 IO Sink Current Notes

When IO pins are used to drive external circuits, follow the absolute maximum current ratings specified in the datasheet, including but not limited to:

(1) IOL: Minimum standard sink current.

(2) IOH: Minimum standard source current.

(3) IOLS: Minimum strong sink current.

(4) IOHS: Minimum strong source current.

Exceeding the absolute maximum ratings may damage the MCU. Device behavior outside the specified range is not guaranteed, and long-term operation beyond the ratings may reduce reliability.

2.9 Protection for Exposed Ports

Communication ports require ESD protection. A small 100Ω series resistor may be added to the signal line to limit ESD current. A Transient Voltage Suppressor (TVS) diode may also be placed in parallel on the signal line, close to the connector.

Programming ports have hot-plug risks and must be protected. During connection, GND should make contact first, followed by IO.

3 Software Application Notes

3.1 GPIO Operation Notes

(1) Unused GPIO ports must be configured by software as low-level outputs.

(2) Before entering low-power mode, set the I/Os to analog mode, disable pull-up and pull-down resistors, select the lowest speed, and set the output registers low.

(3) Do not assign the same alternate function to different GPIO pins!

(4) When VDD is between 0V and 2.7V during power-up, the GPIO ports are floating inputs, and their levels depend on external pull-up or pull-down circuits. Consider the impact on downstream circuit stability. When VDD rises above 2.7V and the power-on reset is complete, the GPIO ports follow the program settings.

3.2 FLASH Erase/Write Notes

(1) PFLASH and DFLASH can be erased separately or together. A single full erase takes approximately 10ms, a combined erase takes approximately 20ms, and a single page erase takes approximately 4ms.

(2) During consecutive multi-page erase operations, clear the watchdog counter as required to prevent a watchdog reset caused by the extended erase time.

(3) Ensure that the power supply remains stable during FLASH erase/write operations. Power instability, including power loss, may cause the FLASH module to malfunction and generate errors. This can lead to ECC errors when the affected FLASH address is accessed after the next power-up. Consider adding voltage monitoring in software to stop FLASH operations when the supply voltage is too low.

(4) After power-up, wait 100ms before operating PFLASH or DFLASH.

(5) Enable the ECC error interrupt. In the interrupt handler, erase the FLASH address that caused the access error to restore access to that address.

(6) After an ECC error occurs, the affected data must be erased. To prevent data loss, use a second FLASH sector as a backup. After writing one sector, also write the same data to the backup sector. The backup sector should be read-only at power-up or when an ECC error occurs. Identify which FLASH sector caused the ECC error and erase that sector. A software flag may be set before reading the address to help identify the source sector.

3.3 FLASH Protection Notes

Read protection is configured through the option byte READPROT at 0x1FFFF800. Three levels are available: 0, 1, and 2. Level 1 enables read protection. Level 2 provides the highest protection level. Once Level 2 is set, the SWD function is permanently disabled and cannot be recovered. Configure this level with caution.

Write protection is configured through option bytes WRP0–WRP7. Each PFLASH bit protects 8KB, and each DFLASH bit protects 1KB.

FLASH read protection and write protection are configured independently. Removing write protection does not erase the main storage contents; the data is preserved.

When writing multiple double-words consecutively, do not cross the half-page boundary. For example, when writing consecutively to PFLASH page 0, the write address must not cross 0x0800 0100.

4 Debugger/Programmer Tool Notes

4.1 Supported Development Environments: IAR, KEIL, Eclipse

(1) IAR: Version 8.50.10 or later is recommended.

(2) KEIL: MDK-ARM V5.36 is recommended.

Note: Projects that failed to compile with an older MDK version may still fail after upgrading. Re-extract the SDK package and use a fresh project copy.

(3) J-Link: Version 9.30 or later is recommended.

(4) Version 2020-12 (4.18.0) or later is recommended. The Eclipse installer can be downloaded from the Eclipse website.

(5) During debugging, confirm that the debug tool supports 5V and uses the same voltage level as the MCU. If needed, provide a 5V reference voltage to match the levels.

4.2 Tool Compatibility

Compatible programming tools include, but are not limited to, the following vendors: Xeltek (SUPERPRO 7500N), PE Micro (CYCLONE), ICW, Sinaen, MaxWiz, DediProg, JinPeng, XuanWei, XinYuan, and XiWei (RongXiang).

4.3 Production Assembly Notes

(1) Always power off the production fixture before placing or removing chips.

(2) Follow proper ESD handling procedures. Do not touch the chip with bare hands.

5 Revision History

Table 1 Document Revision History

Date	Version	Revision History
May, 2026	1.0	● Initial release
June, 2026	1.1	● Added notes and illustrations for NRST circuit modifications ● Added GPIO operation notes ● Added notes on IAR, KEIL, and Eclipse support

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